# Innovations in Infrared Scene Simulator Design

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***Abstract*** ***The MIRAGE (Multispectral Infrared Animation Generation Equipment) Dynamic Infrared Scene Projector, is a joint project developed by Santa Barbara Infrared, Inc. and Indigo Systems Corporation. MIRAGE is a complete infrared scene projector, accepting 3-D rendered analog or digital scene data at its input, and providing all other electronics, collimated optics, calibration and thermal support subsystems needed to stimulated a unit under test with high-fidelity, dynamic infrared scenes. At the heart of MIRAGE is a 512 x 512 emitter array, with key innovations that solve several problems of existing designs. The read-in integrated circuit (RIIC) features "snapshot" updating of the entire 512x512 resistive array, thus solving synchronization and latency problems inherent in "rolling-update" type designs, where data is always changing somewhere on the emitter array at any given time. This custom mixed-signal RIIC also accepts digital scene information at its input, and uses on-board D/A converters and individual unit-cell buffer amplifiers to create analog scene levels, eliminating the complexity, noise, and limitations of speed and dynamic range associated with external generation of analog scene levels. The proprietary process used to create the advanced technology micro-membrane emitter elements allows a wide choice of resistor and structure materials while preserving the dissipation and providing a thermal time constant of the order of 5ms. These innovations, along with a compact electronics subsystem based on a standard desktop PC, greatly reduce the complexity of the required external support electronics, resulting in a smaller, higher performance dynamic scene simulator system***.

## 1. ISSUES WITH CURRENT GENERATION SCENE PROJECTORS

After a considerable investment of time and funds by the infrared test community, several very successful approaches to large array infrared scene simulators using resistive arrays have emerged and been developed into working test systems. Pioneering work by teams from industry and government laboratories[1,2,3] has produced projectors with arrays of up to 544 x 672 pixels. While today's projectors often produce excellent results, a host of problems and difficulties remain for those working with these systems. Building on a large body of previous work and taking to heart lessons learned in the laboratory, a team from Santa Barbara Infrared, Inc. and Indigo Systems set out to build a new projector architecture. During the early stages of the design of the MIRAGE system the team identified and analyzed a number of issues and problems that users have encountered with existing resistor array projection systems. Many of these problem areas were then addressed in the basic design outline of the MIRAGE system. These issues can be grouped as emitter issues and systems issues.

Emitter issues and problem areas that the MIRAGE design team identified include:

1. Difficulties of emitter signal interfaces.
2. The limited selection of array resistor material.
3. Stability of un-annealed resistors
4. Scene dependent image non-uniformity.

System issues include:

1. Lack of standardized Non-Uniformity Correction.
2. Synchronization of emitter frame production and unit under test (UUT) imaging.

**Emitter Issues**

The present generation of very large array infrared scene simulators are all based on arrays of small resistors driven by a read-in integrated circuit. While the sizes of the resistors, the circuit details of the RIICs, and the manufacturing processes vary from supplier to supplier, these systems all have one thing in common. The emitter arrays must be driven with analog voltages, in fact, multiple channels of analog voltages. The analog inputs are sampled by circuits in the RIIC pixel cells at the appropriate time to update individual scene elements. Another common feature of current generation scene simulators is that they must work with digital scene input. The scenes that these devices project are quite often fabricated artificially, using specially adapted 3-D imaging technology, based on high-speed computers. Thus, the interface between the scene projector and the system that generates the images it projects is a digital interface. Since current emitter arrays are inherently analog devices, digital to analog converter (DAC) circuits must be incorporated into scene projector systems. Another fact of life for infrared scene projectors is that virtually all of today's IR simulators are installed in Hardware in the Loop (HWIL) test systems. These systems provide for movement between the unit under test (UUT) and the projected image with multi-axis full-motion simulation systems. Often test requirements dictate that that the emitter projection assembly must be mounted on one motion simulation system while the UUT is mounted on a separate motion system. The requirement for use in the HWIL laboratory is in direct conflict with the analog nature of present emitters. As with any high-resolution DAC application the DAC output and the emitter analog input are ideally placed in extremely close proximity to avoid noise pickup and grounding errors. Since mass must be limited on motion platforms, the system integrator is faced with somehow reducing the mass or number of multiple, bulky DAC circuits, or carefully cabling multiple high-resolution signals from remotely-mounted DACs up to the emitter. The problem becomes more severe at higher frame rates as present generation emitter technology requires more and more analog inputs to support higher frame rates. Thus the system integrator is faced with driving up to 64 analog inputs[3] to get the maximum frame rate performance from the latest arrays. Scaling of arrays to ever-larger formats demanded by the increasing number of pixels in new infrared detectors increases the integrator's challenge exponentially. While the size and complexity issues may be the most obvious drawbacks of present projector systems there are issues with the arrays themselves that hinder high performance projection.

Emitter resistor material has been a subject of considerable development and discussion. The ideal emitter resistor would operate over an extremely wide temperature range with no temperature coefficient. It would also be very durable and possess very high long-term stability, that is, its resistance value would remain constant after many temperature cycles. Current emitter fabrication schemes place formidable

impediments in the way of achieving resistor performance close to this ideal. While all present generation emitters are fabricated with separate, proprietary processes, these processes have one thing in common: their resistors are fabricated on top of a silicon RIIC substrate. Not only must the resistor material and the resistor support material be compatible with silicon processing, but the temperatures used in the fabrication of the resistor must be compatible with the silicon IC itself. This places severe constraints on the choice of resistor materials. Many promising materials must be bypassed because they are not compatible with the silicon processing steps that are required to build the resistor onto the RIIC. Another obstacle is temperature. Finished current generation emitter arrays cannot be bulk annealed at high temperature by baking (the usual method) because the aluminum interconnect used on the IC starts to diffuse into the silicon above about 450°C. Un-annealed resistors have poor long-term stability, and indeed the unrelieved stress of the resistor material may cause non-uniform deformity of resistor microstructures. While it may be possible to anneal resistors by selectively operating portions of the emitter array at higher than normal temperatures for extended periods, this process requires a significant drive voltage overhead on the emitter RIIC, cutting into useful scene dynamic range and reducing accuracy.

At the system level, non-uniformity correction of emitter array projectors continues to be an elusive goal, and MIRAGE system solutions will be discussed in the next section. However, certain contributions to non-uniformity stemming from emitter design are not proper candidates for system level non-uniformity solutions. These contributions to non-uniformity are really RIIC design issues, specifically non-ideal electrical behavior of emitter power bussing. Voltage drops along RIIC power distribution busses, a phenomenon sometimes called bus robbing in current designs, lead to scene dependent non-uniformity as power demands vary with scene commanded intensity changes. Some novel attempts to minimize this effect have been implemented but the remaining scene dependencies still remain for removal by system designers. Unfortunately this is a problem approaching the order of difficulty of scene generation itself.

**System Level Issues**

The difficulty of emitter array non-uniformity correction has been touched upon, and it is sufficient to say that the correction of non-uniform response of emitter resistors remains a topic for further development. System solutions proposed to date have traded simplicity for accuracy[5] or have required large, complex signal processing systems with custom-built data acquisition components[6].

Synchronization of the UUT and the scene projector is a key area of concern. This arises directly from the way in which the present generation emitter arrays update with respect to time. In a current generation array each pixel is updated once per frame period with a new analog voltage which is sampled and then held by the pixel unit cell electronics. The emitter resistor is given the new voltage immediately and begins to change temperature immediately if the new value is different from last frame's voltage. This is shown in the timing diagram of Figure 1, which is a timing diagram of a small, hypothetical current generation emitter array with 20 rows of pixels. For this illustration we will assume that all the pixels in one row of our array are updated together and change at one time. As each row of new scene data is read in to the array, there is a short time where the row sample-holds change, and a longer period of time where the radiance output from the pixels in the row settle to the commanded value. Note that the rows are updated sequentially and at the end of the update period there is a brief time period where the entire image does not change. It is at this time, while the entire image is stable, that UUT integration should occur. Note that in Figure 1 the emitter is not operating at it's maximum frame rate since there is

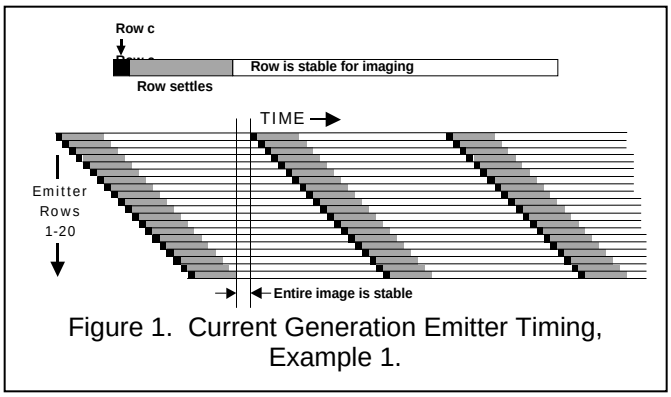

Figure 1. Current Generation Emitter Timing, Example 1.

some delay between the last row change and the start of the next frame at the first row. If a higher frame rate is required this delay can be reduced, resulting in the system timing of Figure 2.

As shown in Figure 2, at a higher frame rate the time during which the array is completely stable is eliminated. Where in Figure 1 there was a short time of image stability after the last frame settled, we can search for that time in vain in Figure 2 for the whole of time period T1. During T1, only the last row is fully stable. and intensities from a new frame are reading in and settling in the upper rows. If we move the UUT integration time to immediately after the last row changes, we still have some of the upper part of the array changing as shown in time period T2, Thus, although this example system may be able to read in scene data at higher frame rates, there is no time during which the unit-under-test can observe an unchanging, settled image. While a snapshot mode UUT such as a high performance staring seeker will be able to freeze the displayed image of Figure 2 temporally, there will always be elements from two different scene frames in the image, complicating the temporal aspect of simulation. This situation can be exacerbated with staring UUTs that themselves have a "rolling update" integration or scanned systems[7].

## 2. MIRAGE SOLUTIONS

As the MIRAGE design team tackled the issues described above, the overall goal was to be able to offer laboratory projection systems that were accurate, reliable, easy to integrate into test facilities, relatively easy to use, and reasonably priced. A further design requirement was to insure that the MIRAGE system could be offered as a standard product at considerable cost savings. While much attention was focused on the emitter, both in its design and the manufacturing process used to fabricate it, other aspects of system function and design were also carefully addressed

### Emitter

The MIRAGE emitter is very much like the current generation of micro resistive emitter arrays in some key aspects. Specifically, MIRAGE resistors are three-dimensional structures suspended over RIIC drive cells, with the one IC cell per pixel. (see Figure 3). There are, however, four significant departures in the design of the MIRAGE emitter. The first is in the fabrication of the array. The current generation of arrays are made by building up resistors on top of a CMOS RIIC via one of several proprietary processes. The MIRAGE emitter, by contrast, is built in two pieces, much like a hybrid infrared detector. One of the pieces is the resistor array and other the CMOS RIIC These separate pieces are then combined using a new proprietary process developed by Rockwell Science Center/Boeing, Thousand Oaks, CA (RSC). The

process, which is called TTFM, mates the resistor array to the RIIC, aligning the resistors and the RIIC, and securing the electrical connections between pixels and the RIIC pixel unit cell. A major advantage of TTFM is that emitter resistors do not have to undergo extensive CMOS IC processing, which means that

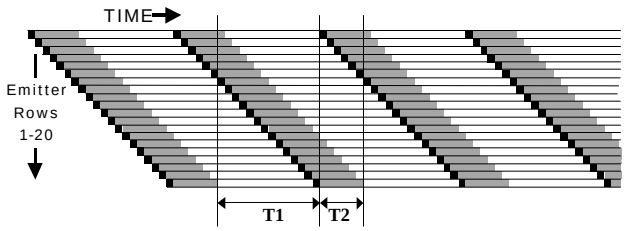

Figure 2. Current Generation Emitter Timing, Example 2.

there are few restrictions on the choice of resistor material. In fact the MIRAGE design team has been able to use the substantial experience base of the commercial resistor fabrication community in selecting materials with the appropriate stability and temperature range for MIRAGE emitter applications. An additional advantage is that any resistor manufacturing steps that require chemistry or temperatures incompatible with the silicon and aluminum of the RIIC are not difficulties with the TTFM process.

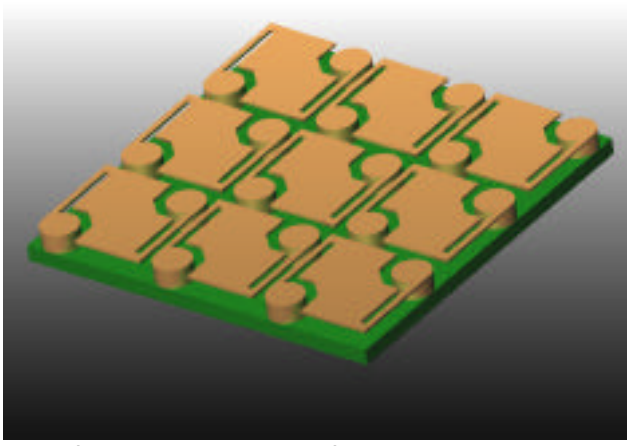
Figure 3. MIRAGE Emitter Array Structure.

This means that emitter arrays can be annealed by baking prior to mating with the RIIC, thus providing emitter resistors with superior stability and relieved stress. The flexibility of TTFM will also allow tailoring of the resistor material to the application in those cases where users prefer a custom resistor solution. There are a number of additional key innovations in the MIRAGE RIIC design as well.

The current generation of emitter RIIC's are very large, but not particularly complex circuits. All examples of RIIC's to date have relied on analog pixel voltages generated from digital pixel data via

multiple DAC circuits located outside of the RIIC. Most emitter RIIC's have been made with previous generation (or older) CMOS fabrication technology. The MIRAGE design team, on the other hand, has leveraged the considerable mixed signal design experience of the infrared detector community in the creation of a large, highly complex, state-of-the-art mixed signal RIIC. This CMOS circuit is designed for fabrication on a standard commercial 0.6um feature size, triple metal process available from a number of silicon foundries worldwide. Two of its key features borrow from work done with staring focal plane read-out IC's for IR detectors; DACs on board the RIIC and "snapshot" mode of pixel unit cell operation. The MIRAGE emitter pixel data port is not an analog input but a pair of 16 bit digital data ports. Pixel data values are read-in, two pixels at a time, and then converted to analog emitter resistor drive levels on the RIIC. The MIRAGE RIIC contains two on-chip high-speed 16-bit DAC circuits of a unique, proprietary design. Since the pixel data stream through the entire

| | |
|---|---|
| Array Size | 512x512 pixels |
| Pixel Size | 39 x 39um |
| Pixel Fill Factor | 46% |
| Response Time Constant(rise) | 4.7ms |
| Response Time Constant (fall) | 5.2ms |
| Dead pixels | less than 0.1% |
| Maximum Actual Pixel Temperature | 600 degrees C above substrate |
| Noise Equivalent Step, Tapp 22C, 3-5um | 4mK |
| Typical Apparent Emitter Output Range (3-5um) | 11 C to 450 C |
| Typical Apparent Emitter Output Range (8-12um) | 10 C to 330 C |
| Apparent Minimum Step Size, Tapp -22C, 3-5um | 3mK |
| Apparent Minimum Step Size, Tapp -300C,3-5um | 24mK |

Table 1. Summary of MIRAGE Emitter Performance

MIRAGE system from scene data input to the emitter remains digital all the inherent noise and crosstalk rejection of digital data and digital data transmission are retained. As with previous generation maximum frame rates are affected by the number of input ports. However, the MIRAGE design anticipates the highest frame rate demands of users by providing two 16-bit digital input ports. Two RIIC data ports supply enough bandwidth to support frame rates as high as 200 frames per second. It should be noted that the pixel unit cell circuit design is such that sampling noise does not increase with frame rate, so use of the full frame rate of 200 frames per second does not incur a noise penalty. Other system implications of all digital operation are discussed below.

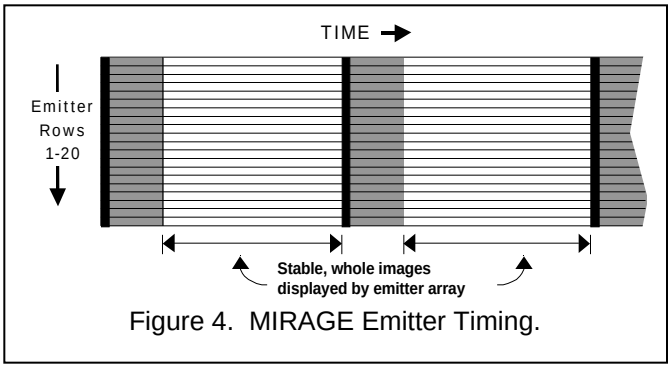


Figure 4. MIRAGE Emitter Timing.

A design goal of the maximum flexibility in image synchronization led to the next RIIC innovation. The pixel drive unit cell in the MIRAGE RIIC uses a novel circuit to allow simultaneous update of all of the emitter pixels at one time. The system benefits of this mode of operation are shown in Figure 4. During a frame update period between the vertical dark lines, data is read in to the emitter in the manner previously described for a hypothetical 20-row emitter in Figures 1 and 2. In Figure 4, the change in the actual emitter drive is delayed until all of the frame's data has been read in. The system benefit is that there is a

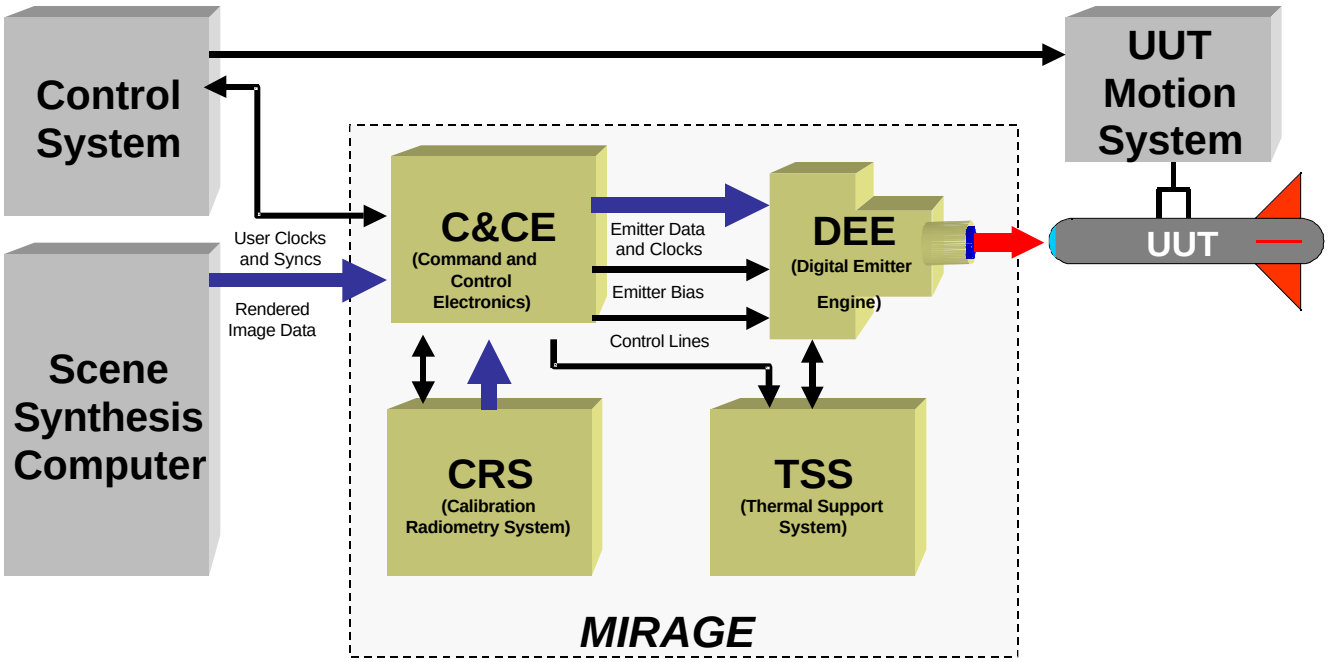

Figure 5. MIRAGE System Block Diagram

long period of time where each frame's image is stable. At high frame rates all pixels settle together, and the UUT can be most effectively synchronized just before the next simultaneous frame change begins. This "Snapshot" mode is selectable, and the "rolling" update mode is also available with the MIRAGE emitter. For scanned systems or staring systems with rolling integration time where the integration time can be accurately controlled, the MIRAGE emitter array will be update in the "rolling update" manner shown in Figures 1 and 2.

A fourth innovation in the MIRAGE RIIC is in the handling of scene dependent local changes in emitter output. The MIRAGE design team attacked this problem in several different ways with the result being a number of unique circuit innovations, each of which is proprietary and subject to future patent. The net result of this IC system approach to crosstalk and noise performance of the MIRAGE emitter is two-fold. On the unit cell level, that is, the circuit that is under each pixel, the power supply noise immunity is improved dramatically. Indeed, noise and other electronic crosstalk effects are reduced to less than the pixel unit cell circuit noise. From system standpoint the entire emitter shows virtually no scene induced image fluctuation and substrate shift. Furthermore, the collection of these circuit advances lead to unique power handling by the RIIC, and the emitter power supply design task is simplified.

The MIRAGE emitter, through innovative RIIC design and resistor manufacturing takes emitter functional integration to new levels, and it also provides considerable performance enhancements. A summary of the MIRAGE emitter specification is shown in Table 1.

**System Solutions**

The MIRAGE emitter is one part of a full system that provides a number key improvements in projector integration and ease of use. The MIRAGE system is shown in the block diagram of Figure 5. The major subsystems include the Digital Emitter Engine (DEE), the Command and Control Electronics (C&CE), the Thermal Support Subsystem (TSS), and the Calibration and Radiometry Subsystem (CRS). The DEE includes the emitter in a vacuum dewar and a small close support electronics package, integrated into the users optical system. The C&CE is the data and control interface of the system, and includes the emitter timing electronics and signal processing electronics. The TSS is a service unit for the DEE that includes a chiller for liquid cooling of the emitter heat sink and a vacuum pump for periodic pump down of the emitter vacuum dewar. The CRS contains an infrared camera, reference blackbodies and an optical system designed to mate with the DEE. The CRS is connected to the C&CE to provide data acquisition for non-uniformity correction coefficient generation and system radiometric calibration. Each of these subsystems is described in detail below.

**DEE**

Since the DEE is the system element that is mounted on a full-motion simulator in an HWIL environment, the goal of the DEE design is to minimize package size and mass, and reduce the complexity of cables that must be brought up to DEE from other system elements. The DEE is where the very high functional integration of the MIRAGE emitter RIIC design is used to maximum advantage. Since the MIRAGE RIIC has on-board DAC circuitry, digital data is brought directly to the DEE. The MIRAGE emitter data input ports, unlike current designs, are not elements of large-geometry analog circuits and have none of the present generation's pickup and noise sensitivity problems. The superior-noise immunity of digital transmission and the flexibility of digital cabling ease the integration of the DEE onto HWIL motion systems. The relatively small emitter housing, in addition to an emitter thermal interface described below, incorporates a high performance vacuum enclosure system with an interchangeable window. The vacuum enclosure is designed to hold vacuum during system operation. Since it is not necessary to pump the DEE vacuum enclosure continuously while the emitter is in operation, there is no need to include a vacuum tube in the permanent cable bundle that connects to the DEE. The TSS can be brought to the DEE and connected to a vacuum nipple on the DEE housing to pump the dewar vacuum shortly before each operation session. The DEE must also interface with the projector's collimating optics and shares a common housing with the optical system

The DEE thermal management system removes heat from the emitter and controls the emitter's substrate during scene projection. The back side of the MIRAGE emitter is bonded to a thermally conductive substrate. The other side of the substrate is connected to a liquid cooled heat sink. A small heater is used for fine control of substrate temperature. Two thermal sensing diodes with integrated current sources and amplifiers on the emitter RIIC provide for measurement of emitter substrate temperature, and this measurement is used for closed loop control of the trim heater.

The DEE contains a small support electronics package for the emitter called the close support electronics. This includes four basic elements; local power regulation of the emitter power supplies and biases, thermal sensor conditioning, sensor communications interface, and pixel data communications

termination. While trim heater power control is handled remotely from the C&CE, the on-RIIC sensor diodes and other optional temperature sensors which might be included in portions of the projector optics are handled with a compact, self-contained, Santa Barbara Infrared Series 2000 off-the-shelf conditioning and measurement subsystem. The standard emitter clock and data interconnect system between the DEE and the C&CE is a fiber optic link which carries all emitter clocks and two 16-bit channels at the maximum frame rate of 200 frames per second. The close support electronics handles the DEE data interface, providing level shifting and fiber optic interface of control and data signals received from the C&CE.

**C&CE**

The C&CE is the system interface and control point. It remotely controls the operation of the other subsystems and provides the control and data interface for both synthetic scene data and projector control and emitter timing and data. The C&CE is based on a standard industrial PC running the Windows NT operating system. Interfaces to the emitter, scene data, UUT synchronization and HWIL laboratory control are managed through a custom PCI bus electronics circuit board that is installed in the C&CE computer. A standard digital data interface is included with the custom electronics of the C&CE as the primary external scene data interface. An off-the-shelf image capture card for standard analog video provides for using either NTSC or PAL video as a secondary source of emitter scene data. The C&CE manages control of other system elements through RS-232 serial links. For MIRAGE systems that include the CRS, the C&CE computer includes an off-the-shelf digital data capture card connected to the CRS IR camera, while the CRS mechanical and blackbody elements are remotely controlled via RS-232 signals. As part of the design goal of ease of interface the C&CE provides a flexible control interface to other elements in the system. MIRAGE timing and emitter operation can function as a slave to another system, as a master to other systems in the laboratory or as a standalone system when displaying analog video input or test patterns. Considerable flexibility in UUT synchronization is also designed into C&CE electronics, allowing a wide variety of UUT sensor systems to successfully operate with MIRAGE.

A Windows NT compliant control program manages the C&CE hardware and various remote interfaces to other system elements. The program provides system status monitoring and a local user control interface. The software package also includes full control, data collection management and non-uniformity coefficient calculation for the CRS. In normal operation the C&CE software package functions include real-time features that constantly monitor the operation of the MIRAGE emitter. The monitor function is the primary element of the emitter safety system that checks on the health and proper operation of the emitter support elements such as the chiller, power supplies, vacuum, and emitter temperature sensors. Proper operation of these system elements must be confirmed before the software monitor will allow powering the emitter, and constant checks of these systems continue in the background during emitter operation.

The high functional integration of the MIRAGE emitter is complemented by the high functional integration of the C&CE custom electronics, which implements the bulk of the system control, signal processing and interface functions with a single circuit card. This card in addition to managing emitter timing, scene data interface, emitter data interface and PC bus interface also incorporates pipelined emitter signal processing. The signal processing built into the C&CE electronics include a multi-point non-uniformity correction circuit, emitter safety monitoring features, time response enhancement and global background correction. Signal processing is implemented in fast, high-capacity FPGA circuits, allowing full frame rate, real-time non-uniformity correction.

Standard input interfaces are used in the C&CE wherever possible. To provide the most flexibility in interfacing user equipment, the digital scene data interface is provided on a small circuit board, separate from the main C&CE electronics board. This small board is specific to a particular interface, providing the physical and electrical matching required by that interface in the form of the correct connector, pinouts, logic levels and clock relationships. The interface board translates the specific signals of the external interface to generic C&CE electronics interface requirements and a short cable connects the interface board to the C&CE electronics input. If the user's scene generation interface changes it's a simple matter of replacing the relatively inexpensive interface board and system operation continues. The first input interface circuit board assembly is for the Silicon Graphics DVP-2 interface.

One of the primary functions of the C&CE electronics board is frame buffering and data rate matching between the user's scene generation computer and the emitter. Normally the emitter is operated at a constant update rate, which is usually the highest system emitter frame rate. Lower simulation frame rates are accommodated by oversampling the UUT. The C&CE can buffer a full frame of simulation data before transmitting it to the emitter. Where data latency is a crucial factor in simulation accuracy, such as at the very highest simulation frame rates, a different type of frame timing and input data synchronization can be used for minimum electronics latency. If the incoming scene data rate and the emitter frame update rate are carefully matched, a full frame of scene data need not be fully buffered in the C&CE before it is transmitted to the emitter. The memories used for frame buffers in the C&CE are large FIFO type memories. While these memories do not have zero latency, they require only a few rows worth of data (or enough for data rate matching) be held in the FIFO before readout to the emitter. Thus, in low-latency mode only a few rows of scene data are buffered by the C&CE and new frame data is passed with very little delay from the scene generation computer through the C&CE to the emitter. For example with the MIRAGE emitter in snapshot mode and at a simulation frame rate of 100 frames per second, the emitter can start to display a new frame within 60 microseconds from the transmission of the last word of the new frame from the scene generation computer to the C&CE.

A very large part of the C&CE custom electronics board is a pipelined, multi-point real-time non-uniformity correction circuit. Other signal processing available on the custom electronics card include a background temperature correction circuit and a time-response acceleration circuit. The background corrector adds or subtracts a small value globally from incoming data to compensate for small variations in emitter substrate temperature. The temperature data from the emitter is transmitted to the C&CE where the C&CE CPU computes the required correction. Another circuit, the delta-temperature circuit is included for improving the apparent time response of the basic emitter. While the emitter time response is fixed by the pixel geometry and material thermal conductivity, an apparent reduction in time constant can be achieved by overdriving pixels when their commanded values change. The delta-temperature circuit makes an approximation to the value that would force the pixel to the commanded value in a single frame time. The circuit includes a separate frame buffer which holds all of the pixel values from the previous frame and an approximation generator. Since the value required to overdrive the pixel depends not only on the frame rate but on the absolute level of the commanded step and the value of difference between frames, the circuit has several options for computation of the overdrive level in the approximation generator, some of which are fixed by the C&CE control computer, and some of which are selected in real time.

It should be noted that all signal processing in MIRAGE is optional. Each signal processing circuit can be switched in or out of the signal chain under software command, and look-up tables can be filled with unity tables for straight data pass through. This allows the user to connect the MIRAGE system in an existing HWIL laboratory at the end of the his signal processing chain. All the user's existing signal chain, which may include complex calculations for rotation, scaling, and non-uniformity correction may remain in place, with the MIRAGE system at the end of the chain, passing input data straight through to the emitter without altering it.

**TSS**

The TSS system is a service module for the DEE, built on its own rolling platform. It includes a liquid chiller for emitter heat removal and substrate temperature control, as well as a source of liquid cooling for temperature stabilizing of DEE optical elements, if required. The chiller is operated by remote control and its operation is monitored by the C&CE system software. The vacuum system on the TSS is intended for occasional use rather than constant pumping of the emitter enclosure during operation. Other elements of the TSS include a Santa Barbara Infrared Series 2000 Smart Blackbody Controller used for emitter substrate temperature control and the emitter raw power supplies.

**CRS**

The CRS is the automated data collection subsystem used for gathering the raw data for calculation of non-uniformity correction coefficients for use in the C&CE multi-point, real-time non-uniformity correction signal processing. The CRS is based on a rigid, machined platform onto which are mounted an infrared camera, camera optics, a motion control system and standard Santa Barbara Infrared Smart Blackbodies. The camera is an off the shelf IR camera operating in the user's band of interest. Image data from the camera is captured by the C&CE CPU which connects to the camera's data port via an off the shelf digital capture system that allows capturing streams of camera frames at the camera's full internal bit depth. The camera's optics provide appropriate magnification such that each emitter pixel maps to at least 4 camera pixels, which reduces the effects of camera spatial non-uniformity and dead camera pixels. The camera has a wide-band dewar window, and the spectral response is tailored to the user's specific bandpass with a warm filter that is provided via filter wheel in the optics. In operation the DEE emitter housing is attached to the CRS motion system, focus confirmed and the automated data collection process is initiated under control of the C&CE CPU. For each emitter calibration point the appropriate camera integration time is remotely selected and emitter pixels are illuminated in sequences of mutually exclusive sparse patterns. Multiple image frames are taken over the surface of the array, as the relative position of the DEE and the camera is adjusted with the motion system. Temporal frame averaging is used to reduce the effects of camera noise, and spatial averaging is used to reduce the effects of camera fixed pattern noise and dead pixels. The entire data collection process can proceed unattended until the required coefficients have been calculated.

## 3. TEST RESULTS

In November 1997 RSC delivered two MIRAGE Pathfinder emitters to Santa Barbara Infrared. The MIRAGE Pathfinders have 512x512 pixels, and have been fabricated

| | |
|---|---|
| Resistance Uniformity | ± 3.65 % |
| Average Thermal Coefficient | -0.047% |
| Average Pixel Emissivity | 91.8% |
| Thermal Time Constant (rise) | 4.7ms |

| | |
|---|---|
| Thermal Time Constant (fall) | 5.2ms |
| Dead Pixels | 0.12% |
| Uniformity at Low Input | 0.46% |
| Uniformity at Medium Input | 7.07% |
| Gain Uniformity | 9.8% |

Table 2, MIRAGE Emitter Test Results Summary.

with the RSC TTFM process on a substrate consisting of a silicon fanout with a single layer of aluminum designed to connect the package pads and groups of pixels.

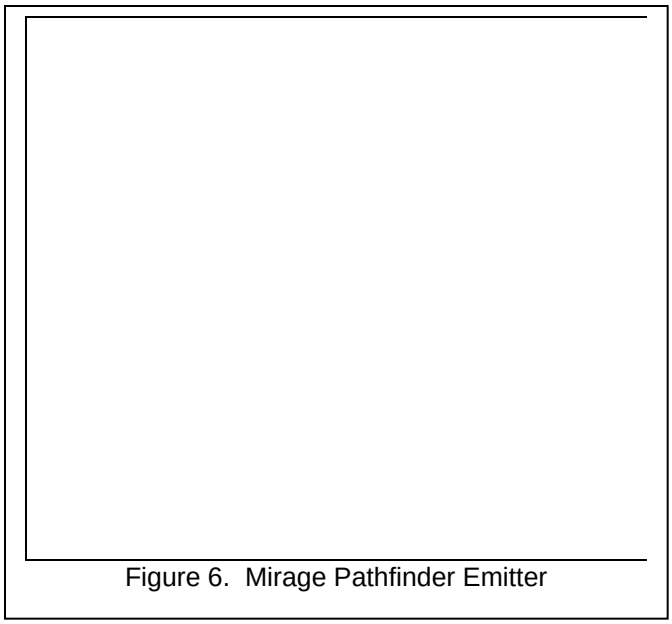

Figure 6. Mirage Pathfinder Emitter

The MIRAGE Pathfinder emitters were delivered in a standard LCC package compatible with a test dewar. Figure 6 is a photograph of one of the MIRAGE Pathfinder emitters. A series of tests were performed by SBIR on the two special devices and Table 2 is a summary of the measurements made to date.

## 4. SUMMARY

A new architecture for an advanced 512 x 512 pixel infrared scene projector has been described. The MIRAGE system incorporates a number of new features that conquer problems and obstacles scene simulation users have encountered in present generation systems. Many of these advances are included directly on the MIRAGE emitter, which offers high functional integration through an advanced, mixed-signal RIIC. The MIRAGE emitter simplifies the emitter interface by incorporating high speed DAC circuitry on the emitter RIIC. This allows for high-resolution digital scene data to be directly connected to the emitter, simplifying cabling, and removing emitter cable length limitations. Other novel design features of the MIRAGE RIIC remove scene-dependent non-uniformity and reduce emitter noise sensitivity. The MIRAGE emitter is built with a new process that allows a wide choice of emitter resistor material and allows resistors to be annealed before assembly. The result is enhanced emitter resistor performance and stability. MIRAGE system flexibility is enhanced by the emitter “snapshot” update mode, which allows all emitter pixels to change at once, and eases synchronization of the MIRAGE system to many UUTs. The full MIRAGE system is itself highly integrated, and in addition to the advanced MIRAGE emitter, includes an electronics control and interface subsystem that implements real-

time non-uniformity correction in a compact package. Full compatibility with existing scene and other laboratory interfaces is maintained in the MIRAGE system, allowing current projector users to obtain many MIRAGE benefits in their laboratories. Finally, the full system flexibility and high functionality of MIRAGE will be offered as a standard off-the-shelf system by Santa Barbara Infrared and Indigo Systems.

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