Scalable Emitter Array Development for Infrared Scene Projector Systems

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ABSTRACT

Several new technologies have been developed over recent years that make a fundamental change in the scene projection for infrared hardware in the loop test. Namely many of the innovations are in Read In Integrated Circuit (RIIC) architecture, which can lead to an operational and cost effective solution for producing large emitter arrays based on the assembly of smaller sub-arrays. Array sizes of 2048x2048 and larger are required to meet the high fidelity test needs of today's modern infrared sensors. The Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training and Instrumentations (PEO STRI) has contracted with SBIR and its partners to investigate integrating new technologies in order to achieve array sizes much larger than are available today. SBIR and its partners have undertaken several proof-of-concept experiments that provide the groundwork for producing a tiled emitter array. Herein we will report on the results of these experiments, including the demonstration of edge connections formed between different ICs with a gap of less than 10μm.

Keywords: Quilting, Tiling, Scalable Array, UHT, Scene Projection, LFRA, MIRAGE XL, WFRA, MIRAGE WF, MIRAGE II, IRSP, pixel.

1. INTRODUCTION

The continued development of larger and larger Infrared Detectors arrays has driven a need for comparably matched test systems using large Infrared Emitter Arrays. The Infrared Scene Projector (IRSP) systems made by Santa Barbara Infrared Inc.(SBIR) have kept pace with this development cycle to date. The introduction of the MIRAGE system at 512x512 emitter pixels was then followed by the Mirage XL[1] system at 10124x1024. Additionally the Wide Format resistive Array (WFRA)[2] program delivered several 1536x768 IRSP systems. The Ultra High Temperature (UHT) [3] scene projector program is striving to reach a producible system with emitter array sizes of 2048x2048 and up to 4096x4096 pixels. With traditional techniques of emitter array fabrication, these array sizes would not be possible. SBIR investigated new developments in Through Silicon Vias (TSVs) as well as Quilt Packaging as a means for creating a composite emitter array fabricated by combining several discrete circuit blocks and then packaging them all as one monolithic device.

Infrared Imaging Systems: Design, Analysis, Modeling, and Testing XXV, edited by Gerald C. Holst, Keith A. Krapels,
Proc. of SPIE Vol. 9071, 90711I · © 2014 SPIE · CCC code: 0277-786X/14/$18 · doi: 10.1117/12.2054360

2. TRADITIONAL METHODS AND YIELD

One of the limitations on the production of large format scene projectors is the yield of the Read-In Integrated Circuit (RIIC) used to control the power to the individual emitters. As the demand for larger pixel format RIICs increases, yield of the RIIC decreases. The MIRAGE-512 and OASIS lines of projectors from Santa Barbara Infrared (SBIR) used RIICs approximately 1 inch (2.5 cm) on a side. Numerous copies of each RIIC die could be placed on a standard 200mm wafer, and yield was typically around 75%. Larger format arrays, such as the SBIR MIRAGE-XL and OASIS 1024[4] arrays with RIICs about 2 inches (5cm) on a side, had substantially lower yield, averaging around 15%. The yield curve projects the cost of the RIIC to be extremely exorbitant and may in fact yield zero at 2048x2048 pixels or larger array size (see Table 1). Based on this analysis, using traditional methods for creating larger and larger emitter arrays would not be economical. Another method must be used to create large arrays. Tiling is one way of producing large format arrays, but traditional tiling is limited by requiring at least one side of a die for circuitry and wire bonds. Maintaining alignment is also a challenge. This is especially true for an emitter array which cannot use post-processing to remove artifacts from the tile seams. To overcome these limitations, SBIR is working towards a four side butt-able or quilted array (tiles) in concert with Through Silicon Vias.

SBIR's concept is to create a RIIC that has all of its Input/Output I/O run through the back of the die using TSVs and then use a process known as Quilt Packaging (QP) to join the arrays with sub-pixel gaps and alignment accuracy. A point on the yield curve is selected that gives an array as large as possible while maintaining good die yield. Based on previous experience as shown in Table 1, a 512x512 array appears to be a good compromise between size and yield. Using QP and TSVs, any format can be assembled based on 512x512 blocks. A new carrier would be required for each new tiled format, but the basic RIIC would be the same, lowering development costs for new RIICs and improving economies of scale in die production.

Table 1. Table of estimated Die Yield Per Array Size

Die Size	Die per 200 mm Wafer	Approximate Yield
256x256	200+	80 – 90%
512x512	50+	75 - 80%
1024x1024	5	10-15%
1536x768	4	10-15%
2048x2048	1	<1%
4096x4096	1 (300mm wafer)	<<1%

3. ARRAY TILING

3.1 Quilt Packaging

Indiana Integrated Circuits, LLC (IIC) researched and designed a fully integrated fabrication process in partnership with Research Triangle Institute (RTI) for post-processing the SBIR RIIC. SBIR wafers will incorporate QP technology for precise chip-to-chip alignment and minimal chip-to-chip gap size. This process combines the micro-electro-mechanical system (MEMS) fabrication currently performed by RTI with the QP process and RTI's through-silicon-via (TSV) technology. Although the complete process has not been performed, IIC and RTI have already demonstrated the feasibility of the individual processes at the RTI facility and have full confidence that the integration approach as-designed, will be feasible for infrared scene projector system needs. Simulation results support the material choices for solder and adhesives, and have reinforced the opinion that there will not be any "show-stoppers" to implementing the full process. Assembly and packaging of the "quilted" array requires modifications to current chip handling

and packaging approaches. In particular, the handling and placement of chips into an arbitrarily large array necessitates improvements to current tools. An analysis of existing equipment options reveals that commercially available systems capable of achieving larger-volume, automated assembly and packaging of arbitrarily large quilted arrays are available. For smaller-volume production, manually operated or partially automated tools are a more economic option. Indiana Integrated Circuits, LLC has developed initial tool designs which were subsequently demonstrated. Using the tools and techniques developed at IIC and RTI, a 2x2 Quilt Packaged demonstrator chip was fabricated.

3.2 Quilt Packaging interconnects

Quilt Packaging is a promising alternative to existing approaches to large format array fabrication. QP offers a robust, affordable, customizable edge-interconnect microchip integration technology. The process utilizes solid metal structures known as "nodules" built into the vertical facet at the edge of the chip. Additionally, the nodules will protrude from the side of the chip, and make electrical and/or mechanical interconnections by mating with equivalent nodule structures on other chips. The result of joining two chips at their edges can be seen in Figure 1, while Figure 2 shows images of individual nodules prior to assembly. With these nodules, a multi-chip "quilt," conceptually resembling sewn panels of a cloth quilt, can be realized. QP is a platform technology, with multiple game-changing advantages depending on the individual system application. QP can deliver sub-micron chip-to-chip alignment, less than 10 micron chip-to-chip gaps, and performs electrically as it were an on-chip interconnect. QP can be implemented in a variety of substrates, enabling heterogeneous integration of disparate materials and/or process technologies for optimal system performance and cost reduction.

A precise, repeatable fabrication process was developed and demonstrated, with chips assembled into 2x2 arrays and key metrics such as alignment and chip-to-chip gap evaluated. Figure 3 illustrates the 3x3 QP array concept.

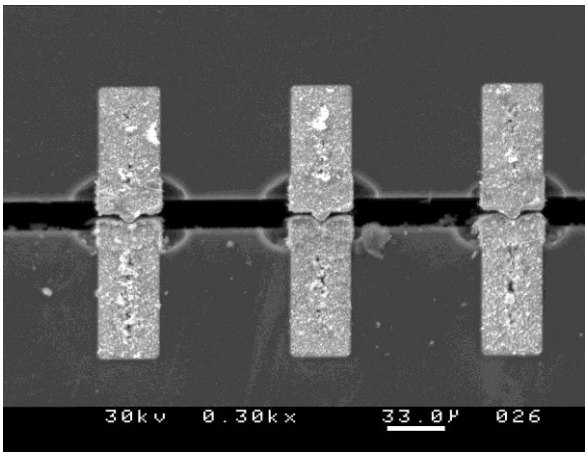

Figure 1. Mated QP nodules, both male and female.

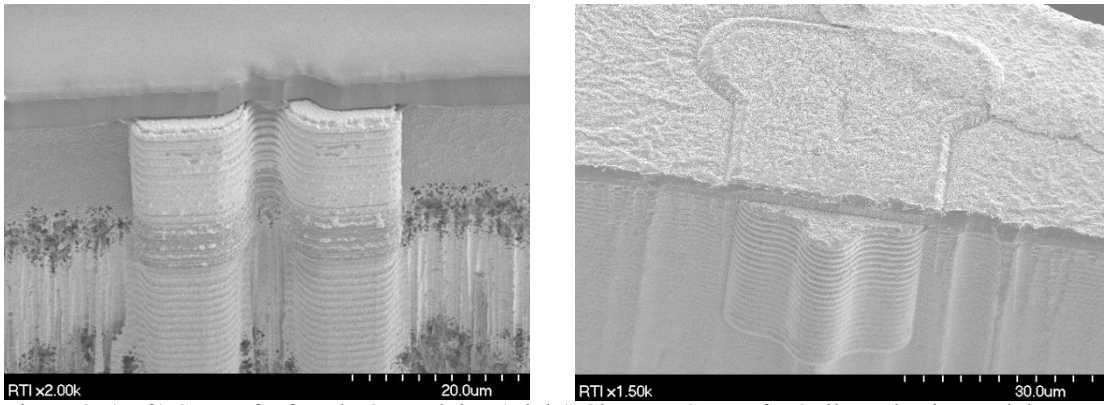

Figure 2. (Left) SEM of a female QP nodule. (Right) Close-up SEM of a Quilt Packaging nodule.

3.3 Electronics & RIIC Integration

Since the QP method can enable arbitrarily large arrays, including 3x3 and hexagonal array concepts, it is possible that a tiled array chip may not have an existing chip edge on the border of the array. In this case, conventional approaches to addressing pixel arrays must be reconsidered. One option is to utilize QP's dense edge I/O characteristics and 10 micron pitch nodule interconnects to complete the signal path chip to chip. Another approach is to utilize Through Silicon Vias and come up from the bottom. The conceptual view of a 3x3 quilted array with back side connections is seen in Figure 3.

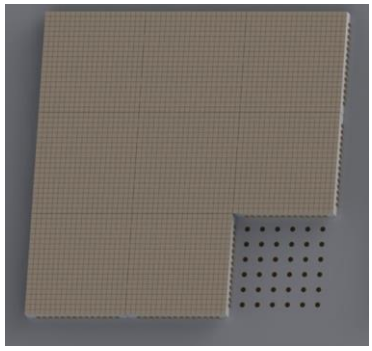
Figure 3. 3x3 quilted array concept

4. THROUGH SILICON VIAS

Conventional read-in integrated circuit (RIIC) designs use a layout approach where a single emitter pixel is replicated N^2 times to create an N×N emitter driver array. Next, wire-bond pads, address decoding circuits, optional digital-to-analog converters, input interface circuits and other support electronics are placed on the periphery of the driver array. A conventional layout approach cannot be used for tiled emitter arrays because there is no room for decoder and I/O circuits on the periphery of the driver array, nor is there room for wire bonds. The application of Through Silicon Via to emitter arrays allows for the rerouting of signal from the bottom of the chip to the top, replacing the connection normally made from the periphery of the chip. By not consuming valuable area on the perimeter of the chip, the active area used can now be expanded to the outer edges of the chip. This allows the chips to utilize the aforementioned Quilt Packaging techniques.

4.1 Through Silicon Vias Chains as Test Vehicle

Through Silicon Vias have been demonstrated by RTI [5] for use with other technologies, but had not been thoroughly demonstrated with thicker wafers and with Quilt Packaging processes. To take the next step in the development of a quilted large format array, a test vehicle was fabricated using both TSVs and QP. A test die, approximately 1 inch on a side with hundreds of TSV chains and QP nodules on the sides was designed and several die fabricated. An scanning electron microscope (SEM) image and optical micrograph of a completed die are shown in Figure 4.

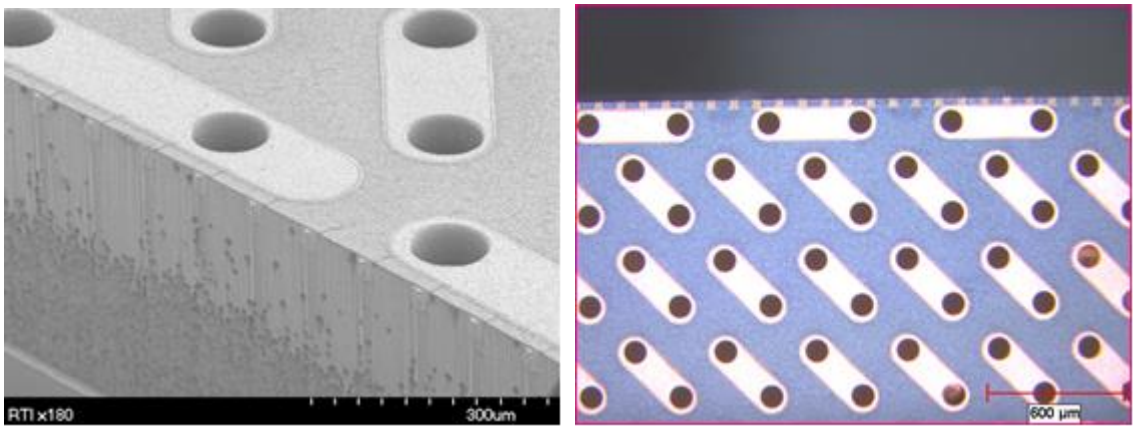

Figure 4. SEM (left) and optical image (right) of a test wafer edge showing Quilt Packaging nodules and Through Silicon Vias.

4.2 First Article Quilt package

QP and TSV technology was successfully integrated on test vehicle, emulating the intended IRSP tiling application. The process compatibility of TSV and Quilt Packaging was demonstrated while some TSV process modifications were made to address issues seen on the first 2 wafers (electrical shorts between chains). However once corrected, the yield of each TSV chain was found to be 100% continuous. Mechanical compatibility of the two interconnect technologies was demonstrated through QP assembly with arrays of 90 µm diameter TSVs set on a 271 µm pitch to their nearest neighbor. No fractures occurred along the TSV rows during handling for qQuilt Packaging assembly. The assembled 2x2 test article can be seen in Figure 5.

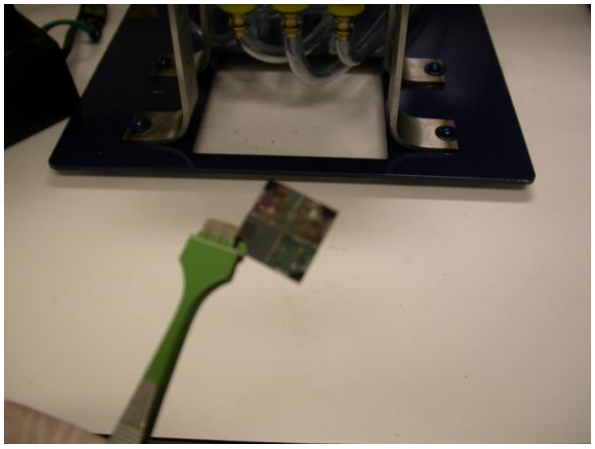

Figure 5. Mechanically stable first article made from 2x2 array of tiles.

The 2x2 test die was mechanically stable able to be held by a single corner and support the entire quilted array. The fabricated gap size of the 2x2 Quilt Packaged test article with Through Silicon Vias was measured to be 11.3 um and can be seen in Figure 6.

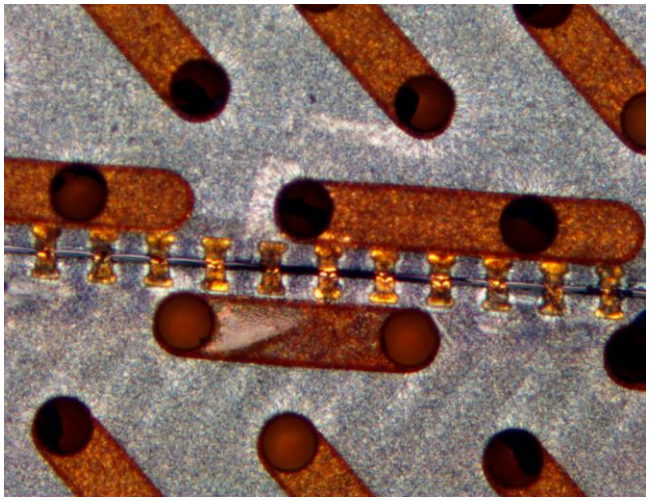

Figure 6. Completed test die with TSV chains and QP nodules. Chip-to-chip gap is 11.3 microns.

5. FURTHER DEVELOPMENT

5.1 TSV Cryogenic operation

The next step in Through Silicon Via development will be to verify that the TSV manufacturing process is capable of functioning at cryogenic temperatures. It is expected that large arrays fabricated using TSVs will be operated at cryogenic temperatures. This extremely cold environment will have an adverse effect on all circuits if they are not designed with this extreme temperature in mind. Experiments are planned that would verify the adhesion of the TSV material to the silicon wall without failure.

5.2 RIIC Chip Carrier Development

The large array is only one part of the overall system. The unique connection properties of the Quilt Packaged emitter array using TSV connections will require that many signals be routed to the underside of the emitter array. To support this connection configuration, a chip carrier capable of routing signals to the underside of the emitter will need to be designed. In addition the unique routing requirements of the chip carrier, it will also need to support much of the off RIIC circuitry that was relocated in order to simplify the RIIC design. The Digital to Analog Converters (DACs) can now be placed on the chip carrier. Having the DACs on the chip carrier allows for the use of commercially available, mass produced, high precision devices from companies like Linear Technologies. The other driving force in the chip carrier design will be the need to support cryogenic operation of the emitter array. The chip carrier will need to be designed to survive the rigors of cryogenic operation much like the OASIS[4] chip carrier designed by SBIR.

6. SUMMARY

The application of Quilt Packaging along with Through Silicon Vias has proven to be viable technologies for creating extremely large arrays for infrared scene projectors in a cost effective manner. Each of these

technologies has been developed further for the unique characteristics of scene projector arrays. Quilt Packaging allows connecting several 512x512 sized tiles to create an arbitrarily large array. Array sizes up to 4Kx4K, or any size based on 512x512 tiles can be fabricated. A 2x2 test article with tiles comparable to 512x512 arrays was fabricated and remained mechanically stable after soldering. The I/O that would normally be routed through the edges can now be routed through the back of the RIIC using Through Silicon Vias. TSVs were developed for the thicker wafers used in IRSPs. Long chains of TSVs were fabricated, tested and showed extremely high reliability and connectivity. Combining these two technologies in an application specific RIIC would allow for the creation of IRSP arrays much larger than what is available today.

DISCLAIMER

This project is funded by the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training and Instrumentation (PEO STRI) under Contract No. W91ZLK-10-C-0009

Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Test Resource Management Center (TRMC) and Evaluation/Science & Technology (T&E/S&T) Program and/or the U.S. Army Program Executive Office for Simulation, Training, & Instrumentation (PEO STRI).

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